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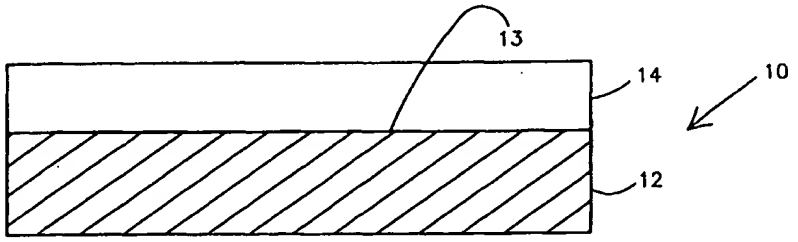

(57) Abstract

A method for use in the fabrication of integrated circuits includes providing a substrate assembly (12) having a surface (13) and forming a barrier layer (14) over at least a portion of the surface. The barrier layer (14) is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995; preferably, x is in the range of about 0.90 to about 0.98. The barrier layer (14) may be formed by chemical vapor deposition and the portion of the surface upon which the barrier layer is formed may be a silicon containing surface. The method is used in formation of capacitors, storage cells, contact liners, etc.

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DIFFUSION BARRIER LAYERS AND METHODS OF FORMING SAME

Field of the Invention

The present invention relates to semiconductor devices and the fabrication thereof. More particularly, the present invention pertains to diffusion barrier layers.

Background of the Invention

In the fabrication of integrated circuits, various conductive layers are used. For example, during the formation of semiconductor devices, such as dynamic random access memories (DRAMs), static random access memories (SRAMs), ferroelectric (FE) memories, etc., conductive materials are used in the formation of storage cell capacitors and also may be used in interconnection structures, e.g., conductive layers in contact holes, vias, etc. In many applications, it is preferable that the material used provide effective diffusion barrier characteristics.

For example, effective diffusion barrier characteristics are required for conductive materials used in the formation of storage cell capacitors of memory devices, e.g., DRAMs. As memory devices become more dense, it is necessary to decrease the size of circuit components forming such devices. One way to retain storage capacity of storage cell capacitors of the memory devices and at the same time decrease the memory device size is to increase the dielectric constant of the dielectric layer of the storage cell capacitor. Therefore, high dielectric constant materials are used in such applications interposed between two electrodes. One or more layers of various conductive materials may be used as the electrode material. However, generally, one or more of the layers of the conductive materials used for the electrodes (particularly the lower electrode of a cell capacitor) must have certain barrier properties and oxidation resistance properties. Such properties are particularly required when high dielectric constant materials are used for the dielectric layer of the storage cell capacitor because of the processes used for forming such high dielectric materials, e.g.,

deposition of high dielectric materials usually occurs at high temperatures (generally greater than about 500° C) in an oxygen-containing atmosphere.

Generally, various metals and metallic compounds, and typically notable metals such as platinum and conductive oxides such as ruthenium oxide, have been proposed as the electrodes or at least one of the layers of the electrodes for use with high dielectric constant materials. However, reliable electrical connections should generally be constructed which do not diminish the beneficial properties of the high dielectric constant materials. For platinum to function well as a bottom electrode, it must be an effective barrier to the diffusion of oxygen. This is required since any oxidation of underlying silicon upon which the capacitor is formed will result in a decreased series capacitance, thus degrading the storage capacity of the cell capacitor. Platinum, used alone as an electrode layer, is too permeable to oxygen to be used as a bottom electrode of a storage cell capacitor.

Because of the permeability of platinum to oxygen, typically platinum is used as a layer in an electrode stack which acts as the electrode as well as a diffusion barrier for integration of capacitors directly formed on silicon. For example, as described in the article "Novel High Temperature Multilayer Electrode-Barrier Structure for High Density Ferroelectric Memories" by H.D. Bhatt, et al., Appl. Phys.Letter, 71(5), 4 August 1997, the electrode barrier structure includes layers of platinum:rhodium alloy, in addition to platinum:rhodium oxide layers, to form electrodes with diffusion barrier properties. Such alloy layers are formed using physical vapor deposition (PVD) processing, e.g., reactive RF sputtering processes.

Many storage cell capacitors are formed using high aspect ratio openings. For example, in U.S. Patent No. 5,392,189 to Fazan, et al., entitled "Capacitor Compatible with High Dielectric Constant Materials Having Two Independent Insulative Layers and the Method for Forming Same," issued February 21, 1995, the storage cell capacitors include a lower electrode that is formed by deposition of a conductive material within a small high aspect ratio opening. Typically, sputtering does not provide a sufficiently conformal layer adequate for formation of an electrode within such a small high aspect ratio opening.

In addition to the formation of capacitor electrodes, the formation of barrier layers for use in other applications, e.g., interconnect applications, is also

desirable. For example, diffusion barriers are commonly used to prevent undesirable reactions in contact openings.

Summary of the Invention

To overcome the problems described above with respect to the use of platinum alone as an electrode material, and others which will be apparent from the detailed description below, a platinum:ruthenium diffusion barrier layer, structures incorporating such layers, and methods associated therewith are described herein.

A method for use in the fabrication of integrated circuits according to the present invention includes providing a substrate assembly having a surface and forming a barrier layer over at least a portion of the surface. The barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995.

In other embodiments of the method, preferably, x is in the range of about 0.90 to about 0.98, and more preferably, x is about 0.95. In another embodiment of the method, the barrier layer is formed by chemical vapor deposition. In yet another embodiment of the method, the portion of the surface upon which the barrier layer is formed is a silicon containing surface.

Another method for use in the formation of a capacitor according to the present invention includes forming a first electrode on a portion of a substrate assembly. A high dielectric material is formed over at least a portion of the first electrode and a second electrode is formed over the high dielectric material. At least one of the first and second electrodes comprises a layer of a platinum:ruthenium alloy.

In one embodiment of the method, at least one of the first electrode and second electrode includes the layer of platinum(x):ruthenium(1-x) alloy and one or more additional conductive layers.

Another method for use in forming a storage cell including a capacitor according to the present invention is described. The method includes providing a substrate assembly including at least one active device and forming a capacitor relative to the at least one active device. The capacitor comprises at least one electrode including a barrier layer of platinum(x):ruthenium(1-x) alloy.

A semiconductor device structure according to the present invention includes a substrate assembly including a surface and a barrier layer over at least a portion of the surface. The barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, wherein x is in the range of about 0.60 to about 0.995.

A capacitor structure according to the present invention includes a first electrode, a dielectric material on at least a portion of the first electrode, and a second electrode on the dielectric material. At least one of the first and second electrodes comprises a barrier layer of platinum(x):ruthenium(1-x) alloy.

A memory cell structure according to the present invention includes a substrate assembly including at least one active device and a capacitor formed relative to the at least one active device. The capacitor comprises at least one electrode including a barrier layer formed of platinum(x):ruthenium(1-x) alloy.

Another integrated circuit structure includes a substrate assembly including at least one active device and an interconnect formed relative to the at least one active device. The interconnect including a barrier layer formed of platinum(x):ruthenium(1-x) alloy.

Brief Description of the Drawings

The present invention will be better understood from reading the following description of illustrative embodiments with reference to the attached drawings, wherein below:

Figure 1 shows a device structure including a platinum:ruthenium alloy layer according to the present invention.

Figure 2 shows a structure including a platinum:ruthenium alloy layer according to the present invention as part of a multiple conductive layer stack.

Figure 3 is a structure including a high dielectric capacitor including an electrode having a platinum:ruthenium alloy layer according to the present invention.

Figure 4 illustrates the use of a platinum:ruthenium alloy layer in a storage cell capacitor application.

Figure 5 illustrates the use of a platinum:ruthenium alloy layer in an interconnect application.

Figures 6A-6C show the results of an example wherein a layer of platinum:ruthenium alloy material is deposited. Figure 6A shows a depth profile of the deposited platinum:ruthenium alloy layer before an oxygen anneal, Figure 6B shows a depth profile of the deposited platinum:ruthenium alloy layer after an oxygen anneal, and Figure 6C shows an XPS montage display showing the Si signal during profile through the platinum:ruthenium layer after annealing in oxygen.

Detailed Description of the Embodiments

The present invention shall be described generally with reference to Figure 1. Thereafter, embodiments and illustrations of applications of the present invention shall be described with reference to Figures 2-5.

Figure 1 illustrates a structure 10 including a substrate assembly 12 and a platinum:ruthenium alloy layer 14 according to the present invention formed on a surface 13 of the substrate assembly 12, e.g., a silicon containing surface. The structure 10 is illustrative of the use of a platinum:ruthenium alloy layer for any application requiring an effective barrier layer. In other words, the platinum:ruthenium alloy layer 14 may be used in the fabrication of semiconductor devices wherever it is necessary to prevent the diffusion of one

material to an adjacent material. For example, the substrate assembly 12 may be representative of a contact structure having an opening extending to a silicon containing surface. In such a structure, diffusion barriers are commonly used in such openings to prevent undesirable reactions, such as the reaction of a contact material, e.g, aluminum, with the silicon containing surface.

Further, for example, the platinum:ruthenium alloy barrier layer 14 may be used in the formation of storage cell capacitors for use in semiconductor devices, e.g., memory devices. As further described herein, the platinum:ruthenium alloy barrier layer 14 may be used alone as an electrode in such storage cell capacitors or within a stack of layers forming an electrode of a capacitor. One skilled in the art will recognize that various semiconductor processes and structures for various devices, e.g., CMOS devices, memory devices, etc., would benefit from the barrier characteristics of the barrier layers of the present invention and in no manner is the present invention limited to the illustrative embodiments described herein.

As used in this application, "substrate assembly" refers to either a semiconductor substrate such as the base semiconductor layer, e.g., the lowest layer of a silicon material in a wafer, or a silicon layer deposited on another material, such as silicon on sapphire, or a semiconductor substrate having one or more layers or structures formed thereon or regions formed therein. When reference is made to a substrate assembly in the following description, various process steps may have been previously used to form or define regions, junctions, various structures or features, and openings such as vias, contact openings, high aspect ratio openings, etc.

The platinum:ruthenium alloy layer 14 according to the present invention includes an atomic composition of platinum(x):ruthenium(1-x), where preferably, x is in the range of about 0.60 to about 0.995. In other words, the amount of ruthenium necessary in the platinum layer to accomplish barrier characteristics for semiconductor devices is minimal, i.e., in the range of about 40% to about .5%. More preferably, x is in the range of about 0.90 to about 0.98; and, yet more preferably, x is about 0.95, i.e., about 5% ruthenium in the layer is suitable to provide barrier characteristics. In other words, preferably, the atomic composition of the platinum:ruthenium alloy layer 14 is about 95% platinum and 5% ruthenium.

The thickness of the platinum:ruthenium alloy layer 14 is dependent upon the application for which it is used. Preferably, the thickness is in the range of about 10 Å to about 10,000 Å. More preferably, the thickness of the platinum:ruthenium alloy layer 14 is in the range of about 100 Å to about 500 Å. For example, this preferred thickness range of about 100 Å to about 500 Å is applicable to a single platinum:ruthenium alloy layer forming an electrode of a capacitor.

The platinum:ruthenium alloy layer 14 formed on the surface 13 of substrate assembly 12 may be formed by one or more various processes. For example, the formation of the platinum:ruthenium alloy layer 14 may be accomplished by the simultaneous evaporation of the metals from respective sources, i.e., co-evaporation; may be sputter deposited from a single deposition target of platinum:ruthenium alloy; may be deposited by the simultaneous co-sputtering from two targets (i.e., one target including platinum and the other target including ruthenium); or may be deposited by chemical vapor deposition (CVD), for example, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), or any other chemical vapor deposition technique. Preferably, the formation of the platinum:ruthenium alloy layer 14 is attained by CVD.

For example, the process may be carried out in a chemical vapor deposition reactor, such as a reaction chamber available under the trade designation of 7000 from Genus, Inc., (Sunnyvale, CA), or available under the trade designation of 5000 from Applied Materials, Inc., (Santa Clara, CA), or available under the trade designation of Prism from Novelus, Inc., (San Jose, CA). However, any reaction chamber suitable for performing CVD may be used.

Chemical vapor deposition (CVD) is defined as the formation of a non-volatile solid film on a substrate by the reaction of vapor phase reactants, i.e., reactant gases, that contain desired components. The reactant gases are introduced into the reaction chamber. The gases decompose and react at a heated wafer surface to form the desired layer. Chemical vapor deposition is just one process of providing thin layers on semiconductor wafers, such as films of elemental metals or compounds, e.g., platinum:ruthenium alloy layers.

Chemical vapor deposition processes are favored in many respects because of the process capability to provide highly conformal layers even within deep contacts and other openings. Thus, as described further below with reference to Figures 4 and 5, CVD processing is preferably used to provide highly conformal layers within deep contacts and other openings such as for lower electrodes of storage cell capacitors. It will be readily apparent to one skilled in the art that although CVD is the preferred process, that the CVD process may be enhanced by various related techniques such as plasma assistance, photo assistance, laser assistance, as well as other techniques.

Preferably, according to the present invention, the co-deposition of platinum and ruthenium is conducted using a CVD process wherein a ruthenium precursor is delivered to a reaction chamber along with a platinum precursor. Preferably, the method is carried out in the presence of an oxidizing reactant gas, such as O_2, NO, N_2O, O_3, hydrogen peroxide, organic peroxides such as T-butyl peroxide, or any other oxidizing agent.

Typically, a liquid precursor is contained in a bubbler reservoir through which a carrier gas, such as helium or any other inert, i.e., nonreactive gas (e.g., nitrogen, argon, neon, and xenon) is bubbled through the reservoir containing the precursor to deliver the precursor to the reaction chamber. For example, a flow of carrier gas having a flow in the range of about one sccm to about 100 sccm of a nonreactive gas, i.e., nonreactive with other gases of the process, is used in a bubbler having a pressure in the range of about 0.5 to about 50 torr and a temperature in the range of about 30° C to about 70° C to deliver a platinum precursor to the reaction chamber. Likewise, a carrier gas, i.e., a nonreactive gas, having a flow in a range of about one sccm to about 10 sccm is used in a bubbler containing a ruthenium precursor at the conditions of about 0.5 torr to about 100 torr and a temperature of about 20° C to about 50° C to deliver the ruthenium precursor to the reaction chamber. Preferably, the reactant oxidizing gas is provided to the reaction chamber at a flow of about 0 sccm to about 500 sccm.

One skilled in the art will recognize that the manner in which the gases are introduced into the reaction chamber may include one of various techniques. For example, in addition to provision by bubbler techniques, the introduction may be accomplished with the use of compounds which are gases at room

temperature or by heating a volatile compound and delivering the volatile compound to the reaction chamber using a carrier gas. Further, solid precursors and various methods of vaporizing such solid precursors may also be used for introduction of reactant compounds into the chamber. As such, the present invention is not limited to any particular technique. Further, typically, the reactant gases are admitted at separate inlet ports. In addition to the reactant gases, a dilution gas (i.e., a gas that is non-reactive with the reactant gases) may also be introduced into the chamber. For example, argon gas may be introduced into the chamber at a varied flow rate.

Therefore, in accordance with the present invention, the reactant gas mixture in the reaction chamber includes at least the ruthenium precursor gas, the platinum precursor gas, and optionally the oxygen reactant gas and/or a dilution gas. Preferably, within the reaction chamber, the partial pressure of ruthenium precursor gas is kept sufficiently low such that the ruthenium deposited is within the ranges described for forming the preferred platinum:ruthenium composition of the alloy layer 14 described above. This partial pressure may be controlled by controlling the flow of the inert gas, e.g., helium, through the bubbler containing the ruthenium precursor or through control of other parameters of the process, such as temperature and pressure of the bubbler.

In the preferred CVD process, the reaction chamber pressure is preferably maintained at a deposition pressure of about 0.5 torr to about 5 torr. The deposition temperature at the wafer surface upon which the platinum:ruthenium alloy layer 14 is deposited is held at a temperature in a range of about 200° C to about 400° C.

Any ruthenium-containing precursor and platinum-containing precursor may be used in accordance with the present invention. Preferably, the platinum containing precursors include $MeCpPtMe_3$ (where Cp=cyclopentadienyl), platinum hexafluoroacetylacetonate, $CpPtMe_3$, $Pt(acetylacetonate)_2$, $Pt(PF_3)_4$, $Pt(CO)_2Cl_2$, $cis\text{-}PtMe_2[MeNC]_2$, $(COD)Pt(CH_3)_2$, $(COD)Pt(CH_3)Cl$, $(C_5H_5)Pt(CH_3)(CO)$, $(acac)(Pt)(CH_3)_3$, where COD = 1,5 cyclooctadiene and acac = acetylacetonate. Further, preferably, the ruthenium precursors are liquid ruthenium complexes of the following formula (Formula I): $(diene)Ru(CO)_3$ wherein: "diene" refers to linear, branched, or cyclic dienes, bicyclic dienes,

tricyclic dienes, fluorinated derivatives thereof, combinations thereof, and derivatives thereof additionally containing heteroatoms such as halide, Si, S, Se, P, As, or N. These precursor complexes and others are described in Assignees' copending patent application entitled "Precursor Chemistries for Chemical Vapor Deposition of Ruthenium and Ruthenium Oxide" having U.S. Serial No. _____ (Micron Docket No. 97-0675) and in Assignees' copending patent application entitled "Methods for Preparing Ruthenium and Osmium Compounds" having U.S. Serial No. _____ (Micron Docket No. 97-0861). Further, for example, additional precursors are generally discussed in U.S. Patent No. 5,372,849 to McCormick et al. More preferably, the ruthenium precursors used according to the present invention include one of $C_6H_8Ru(CO)_3$, bis(cyclopentadienyl) ruthenium (II), triruthenium dodecacarbonyl, and cyclopentadienyl dicarbonyl ruthenium (II) dimer.

Methods of forming the co-deposited platinum:ruthenium alloy layer 14 are described in co-pending patent application entitled "Method for Producing Low Carbon/Oxygen Conductive Layers" (Docket No. 150.00730101 (Micron Docket No. 97-0996). One skilled in the art will recognize that these methods and various other methods may be used to form the platinum:ruthenium alloy layer 14 according to the present invention.

Figure 2 shows a structure 20 including substrate assembly 22 and a stack 24. The stack 24 includes conductive layers 31-34. One or more of the conductive layers 31-34 are platinum:ruthenium alloy layers according to the present invention.

The one or more conductive layers, in addition to including one or more platinum:ruthenium alloy layers, may include conductive layers formed of various conductive materials. For example, the conductive layers may include, but are clearly not limited to, layers formed from metals such as platinum, paladium, rhodium, ruthenium, osmium, and iridium; metal alloys such as platinum:rhodium, platinum:ruthenium, and platinum:iridium; metal oxides such as ruthenium oxide, rhodium oxide, and iridium oxide; metal alloy oxides such as platinum:rhodium oxide, platinum:ruthenium oxide, and platinum:iridium oxide; metal nitrides such as titanium nitride, tungsten nitride, and tantalum nitride; metal silicides such as titanium silicide, ruthenium silicide, rhodium silicide, and iridium silicide.

The stack 24 may be used for one or numerous applications, e.g., interconnection applications, capacitor applications, etc. For example, stack 24 may be used as an electrode for a storage cell capacitor with substrate assembly 22 including a silicon containing surface 23. As such, the barrier properties of the stack 24 must prevent silicon diffusion from silicon-containing surface 23. In accordance with the present invention, the layer 31 may be formed as a platinum:ruthenium alloy layer to prevent diffusion of silicon from silicon-containing surface 23 through stack 24 to adjacent layer or layers 29. Further, for example, in the case where layer 29 is a high dielectric material requiring diffusion barrier properties to prevent oxygen from diffusing through stack 24, layer 34 or one of the other layers may also be formed as a platinum:ruthenium alloy barrier layer according to the present invention. One skilled in the art will recognize that the platinum:ruthenium alloy layer according to the present invention may be used in a stack of layers for a variety of applications and the stack may include one or more platinum:ruthenium alloy layers. Further, the composition of such platinum:ruthenium layers used in the same stack may differ.

Figure 3 shows a structure 50 including substrate assembly 52 and capacitor structure 54. Capacitor structure 54 includes a first electrode 56, a second electrode 60, and a high dielectric constant layer 58 interposed therebetween. For example, the dielectric layer may be any suitable material having a desirable dielectric constant, such as Ta_2O_5, $Ba_xSr_{(1-x)}TiO_3$ [BST], $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$ [PZT], $(Pb,La)(Zr,Ti)O_3$ [PLZT], $(Pb,La)TiO_3$ [PLT], KNO_3, and $LiNbO_3$. With use of the high dielectric constant layer 58, diffusion barrier properties of the electrodes is particularly important. For example, to function well in a bottom electrode of a capacitor structure, the electrode layer or electrode stack must act as an effective barrier to the diffusion of oxygen, particularly due to the processes used to form the high dielectric constant materials. Such diffusion barrier properties are particularly required when the substrate assembly 52 includes a silicon-containing surface 53 upon which the capacitor is formed, e.g., polysilicon, silicon substrate material, N-doped silicon, P-doped silicon, etc., since oxidation of the diffused silicon may result in degraded capacitance, e.g., capacitance for a memory device. The co-deposition of the platinum with the ruthenium enhances the barrier properties of

the layer formed and thus provides a significant improvement over pure platinum for electrode applications.

One skilled in the art will recognize that either of the electrodes 56, 60 may be formed as a single layer of platinum:ruthenium alloy material. Further, such electrodes 56, 60 may be formed as a stack such as described with reference to Figure 2 including one or more layers of a platinum:ruthenium alloy material and one or more additional conductive layers.

Two illustrations of using the platinum:ruthenium alloy layer or layers as described above are shown and described below with reference to Figures 4 and 5. The use of the platinum:ruthenium layer or layers according to the present invention is described with reference to Figure 4 wherein a bottom electrode of a high dielectric capacitor of a storage cell includes one or more layers of the platinum:ruthenium alloy material as described herein. Further, the use of platinum:ruthenium alloy layer or layers according to the present invention is described with reference to Figure 5 wherein a contact liner requiring diffusion barrier characteristics is described. For simplistic purposes, the illustrative descriptions are limited to the use of the platinum:ruthenium alloy material described in these two illustrative structures. There are other semiconductor processes and structures for various devices, e.g., CMOS devices, memory devices, logic devices, etc., that would benefit from the present invention and in no manner is the present invention limited to the illustrative embodiments described herein, e.g., contact liner and electrode structure. The platinum:ruthenium alloy barrier layer may be used for any application requiring diffusion barrier characteristics, particularly those for preventing diffusion of oxygen and silicon into adjacent layers.

As shown in Figure 4, a device structure 100 is fabricated in accordance with conventional processing techniques through the formation of an opening 184 prior to depositing a bottom electrode structure on the surfaces 185, 186 defining the opening 184. A platinum:ruthenium alloy bottom electrode is then formed in opening 184. As such, and as further described in U.S. Patent No. 5,392,189 to Fazan, et al., the device structure 100 includes field oxide regions 105 and active regions, i.e., those regions of the substrate 107 not covered by field oxide. A word line 121 and an active device, i.e., field effect transistor (FET) 122, are formed relative to the field oxide region 105. Suitable

source/drain regions 125, 130 are created in silicon substrate 107. An insulative layer of oxide material 140 is formed over regions of FET 122 and word line 121. Polysilicon plug 165 is formed to provide electrical communication between substrate 107 and the storage cell capacitor to be formed thereover. Various layers are formed over the polysilicon plug 165, including layers 167 and 175. For example, such layers may be titanium nitride, tungsten nitride, or any other metal nitride which acts as a barrier, and may also include one or more platinum:ruthenium alloy barrier layers as described herein. Thereafter, another insulative layer 183 is formed and an opening 184 is defined therein.

The opening 184 is a small high aspect ratio opening. As described herein, small high aspect ratio openings have feature sizes or critical dimensions below about 1 micron (e.g., such as a diameter or width of an opening being less than about 1 micron) and aspect ratios greater than about 1. Such aspect ratios are applicable to contact holes, vias, trenches, and any other configured openings. For example, a trench having an opening of 1 micron and depth of 3 microns has an aspect ratio of 3. The present invention is particularly beneficial for forming diffusion barrier layers in small high aspect ratio features due to the use of CVD processes for forming conformal layers of the platinum:ruthenium alloy material over step structures.

As shown in Figure 4, a platinum:ruthenium alloy barrier layer 187 is formed on the bottom surface 185 and the one or more side walls 186 defining opening 184. A layer of platinum:ruthenium alloy material is first co-deposited over the entire structure including the bottom surface 185 and sidewalls 186 and then formed into lower electrode 187. For example, the layer may be etched or planarized to remove the desired regions for forming the bottom electrode 187. Thereafter, dielectric layer 191 is then formed relative to the platinum:ruthenium alloy diffusion barrier layer 187. Further thereafter, the second electrode 192 is formed relative to the dielectric material 191. For example, such an electrode may be of any conductive material such as the platinum:ruthenium alloy barrier material as described herein, tungsten nitride, titanium nitride, tantalum nitride, ruthenium, rhodium, iridium, ruthenium oxide, iridium oxide, any combination thereof, or any other conductive material typically used as an electrode of a storage cell capacitor. With the use of the present invention, the bottom electrode formed of platinum:ruthenium alloy material is conformally formed of

uniform thickness using CVD within opening 184 providing a desired resistivity and barrier properties.

It will be recognized by one skilled in the art that any capacitor formed relative to a surface, e.g., silicon containing surface, whereupon diffusion barrier properties are required and/or conformally formed conductive layers are required will benefit from the present invention. For example, container capacitors typically includes electrodes formed on surfaces requiring conformal formation of a bottom electrode. Such a container capacitor storage cell is described in U.S. Patent No. 5,270,241 to Dennison, et al., entitled "Optimized Container Stack Capacitor DRAM Cell Utilizing Sacrificial Oxide Deposition and Chemical Mechanical Polishing," issued December 14, 1993. One skilled in the art will also recognize that the bottom electrode 187 may include a stack of layers with one or more of the layers being a platinum:ruthenium alloy barrier layer as described previously herein. As shown in Figure 5, device structure 200 is fabricated in accordance with conventional processing techniques through the formation of contact opening 259 prior to metalization of the contact area 255 of substrate 207. As such, prior to metalization, the device structure 200 includes field oxide regions 205 and active areas, i.e., those regions of substrate 207 not covered by field oxide. Formed relative to the field oxide regions 205 in the active areas are word line 221 and FET 222. Suitably doped source/drain regions 225, 230 are formed as known to one skilled in the art. A conformal layer of oxide material 240 is formed thereover and contact opening 259 is defined therein to the contact area 255 of doped region 230 of silicon substrate 207. Thereafter, one or more metalization or conductive layers are formed in the contact opening 259 for providing electrical connection to substrate region 230. For example, various materials may be formed in contact opening 259, such as titanium nitride or other diffusion barrier materials. Preferably, contact liner 285 is formed of platinum:ruthenium alloy material according to the present invention on bottom surface 260 and the one or more side walls 261 defining the opening 259. The platinum:ruthenium alloy layers are generally deposited over the entire substrate assembly and then planarized to form the contact liner 285. Thereafter, a conductive material 276 is formed in the contact opening for providing connection to doped region 230 of substrate 207.

Example

Figures 6A and 6B show depth profiles of a co-deposited platinum:ruthenium layer before and after an oxygen anneal, respectively. The small lab scale reaction CVD chamber was built by MDC Vaccuum Products Corp. (Hayward, CA) and the glass research bubbler is from Technical Glass Service (Boise, ID). The conditions used for the co-deposition of the platinum:ruthenium layer include:

Platinum Precursor: $MeCpPt(Me)_3$.

Ruthenium Precursor: $C_6H_8Ru(CO)_3$.

Platinum Carrier Gas for use through Bubbler: 5 sccm of helium.

Ruthenium Carrier Gas for use through Bubbler: 10 sccm of helium.

Platinum Bubbler Conditions: pressure of 10 torr, temperature of 33° C.

Ruthenium Bubbler Conditions: pressure of 40 torr, temperature of 25° C.

Reaction Chamber Conditions: pressure of 5 torr, deposition temperature of 300° C at wafer surface.

Deposition Time: 4 minutes.

Oxygen Reaction Gas: 10 sccm.

The depth profile was attained by using an XPS device available under the trade designation of PhI (Φ) 5600 from Physical Electronics (Eden Prairie, MN). The operating conditions for obtaining the profile include x-ray source of 350 W, monochromatic Al k_α (hV = 1486.6 eV); 45 degree extraction; 800 μm extraction aperture. Sputtering was performed with a 4 keV Argon ion beam rastored over a 3 mm area. The sputter time for the depth profile of Figure 6A was 13 minutes and the sputter time for the depth profile of Figure 6B was 14.3 minutes.

As shown in Figure 6A, the co-deposited platinum:ruthenium layer deposited according to the above conditions is shown therein including at a depth of 200 Å a platinum composition of about 70% and a ruthenium composition of about 15%. Figure 6B shows the co-deposited platinum:ruthenium layer after being subjected to a rapid thermal oxidation anneal at 750° C for a period of 30 seconds. Figure 6C shows an XPS montage display showing the Si signal during profile through the platinum:ruthenium

layer, after annealing in oxygen. The peak shape shows the lack of SiO_2 at the interface and only traces of Si at the surface. There appears to be no silicon diffusion or oxygen diffusion through the barrier layer and therefore, no silicon dioxide formation.

All patents and references cited herein are incorporated in their entirety as if each were incorporated separately. This invention has been described with reference to illustrative embodiments and is not meant to be construed in a limiting sense. As described previously, one skilled in the art will recognize that various other illustrative applications may use the platinum:ruthenium alloy layer as described herein to take advantage of the beneficial barrier characteristics thereof. Various modifications of the illustrative embodiments, as well as additional embodiments to the invention, will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments that may fall within the scope of the present invention as defined by the accompanying claims.

What is claimed is:

1. A method for use in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly having a surface; and

forming a barrier layer over the at least a portion of the surface, wherein the barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995.

2. The method of claim 1, wherein x is in the range of about 0.90 to about 0.98.

3. The method of claim 2, wherein x is about 0.95.

4. The method of claim 1, wherein forming the barrier layer includes forming the barrier layer by chemical vapor deposition.

5. The method of claim 1, wherein the portion of the surface is a silicon containing surface.

6. A method for use in the formation of a capacitor, the method comprising:

forming a first electrode on a portion of a substrate assembly;

forming a high dielectric material over at least a portion of the first electrode; and

forming a second electrode over the high dielectric material, wherein at least one of the first and second electrodes comprises a layer of a platinum:ruthenium alloy.

7. The method of claim 6, wherein the layer of platinum:ruthenium alloy is a layer of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995.

8. The method of claim 7, wherein x is in the range of about 0.90 to about 0.98.

9. The method of claim 8, wherein x is about 0.95.

10. The method of claim 1, wherein forming the at least one of the first electrode and second electrode comprising the layer of platinum(x):ruthenium(1-x) alloy includes forming the layer of platinum(x):ruthenium(1-x) alloy by chemical vapor deposition.

11. A method for use in the formation of a capacitor, the method comprising:

providing a silicon containing surface of a substrate assembly;

forming a first electrode on a least a portion of the silicon containing surface of the substrate assembly, the first electrode including a layer of platinum(x):ruthenium(1-x) alloy;

providing a high dielectric material over at least a portion of the first electrode; and

providing a second electrode over the high dielectric material.

12. The method of claim 11, wherein the first electrode is a single layer of platinum (x) and ruthenium (1-x) alloy.

13. The method of claim 12, wherein a thickness of the layer is in a range of about 100Å to about 500Å.

14. The method of claim 11, wherein the step of forming the first electrode includes depositing the layer of platinum (x):ruthenium (1-x) alloy by chemical vapor deposition.

15. The method of claim 11, wherein x is in the range of about 0.60 to about 0.995.

16. The method of claim 15, wherein x is in the range of about 0.90 to about 0.98.

17. The method of claim 11, wherein the first electrode includes the layer of platinum(x):ruthenium(1-x) alloy and one or more additional conductive layers.

18. The method of claim 17, wherein the one or more additional conductive layers are formed from materials selected from the group of metals and metal alloys; metal and metal alloy oxides; metal nitrides; and metal silicides.

19. A method for use in forming a storage cell including a capacitor, the method comprising:

providing a substrate assembly including at least one active device; and

forming a capacitor relative to the at least one active device, the capacitor comprising at least one electrode including a barrier layer of platinum(x):ruthenium(1-x) alloy.

20. The method of claim 19, wherein forming the at least one electrode includes depositing the barrier layer of platinum (x):ruthenium(1-x) alloy by chemical vapor deposition.

21. The method of claim 19, wherein x is in the range of about 0.60 to about 0.995.

22. The method of claim 21, wherein x is in the range of about 0.90 to about 0.98.

23. A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a barrier layer over at least a portion of the surface, wherein the barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995.

24. The structure of claim 23, wherein x is in the range of about 0.90 to about 0.98.

25. The structure of claim 24, wherein x is about 0.95.

26. The structure of claim 23, wherein the portion of the surface is a silicon containing surface.

27. A capacitor structure comprising:

a first electrode;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a barrier layer of platinum(x):ruthenium(1-x) alloy.

28. The structure of claim 27, wherein x is in the range of about 0.60 to about 0.995.

29. The structure of claim 28, wherein x is in the range of about 0.90 to about 0.98.

30. The structure of claim 27, wherein at least one of the first electrode and second electrode comprises the barrier layer of platinum(x):ruthenium(1-x) alloy and one or more additional conductive layers.

31. The structure of claim 30, wherein the one or more additional conductive layers are formed from materials selected from materials selected from the group of metals and metal alloys; metal and metal alloy oxides; metal nitrides; and metal silicides.

32. A memory cell structure comprising:

a substrate assembly including at least one active device; and

a capacitor formed relative to the at least one active device, the capacitor comprising at least one electrode including a barrier layer formed of platinum(x):ruthenium(1-x) alloy.

33. The structure of claim 32, wherein the capacitor includes:

a first electrode formed relative to a silicon containing region of the at least one active device;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein the first electrode comprises the barrier layer formed of platinum(x):ruthenium(1-x) alloy.

FIGURE 1

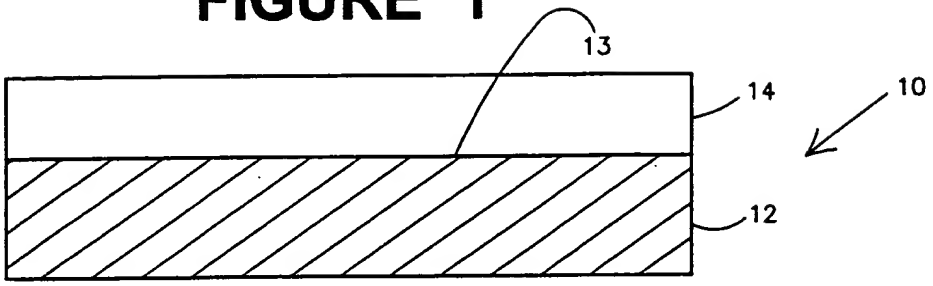


FIGURE 2

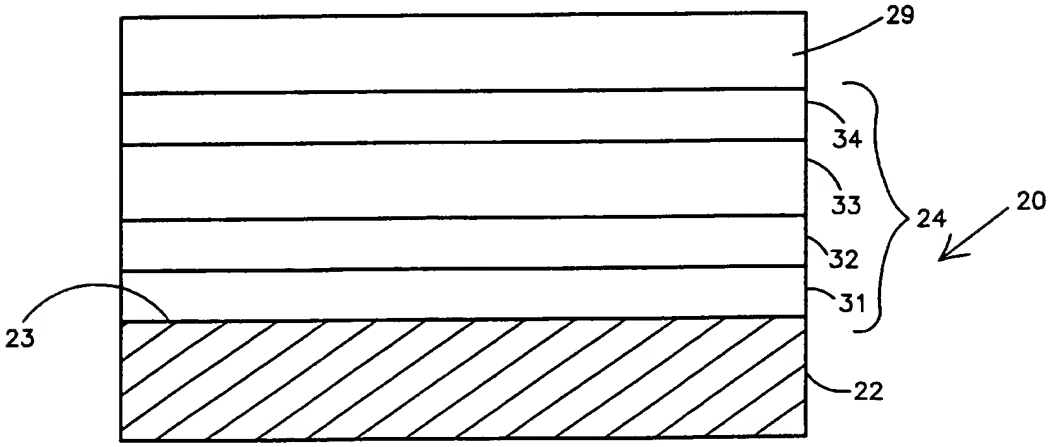


FIGURE 3

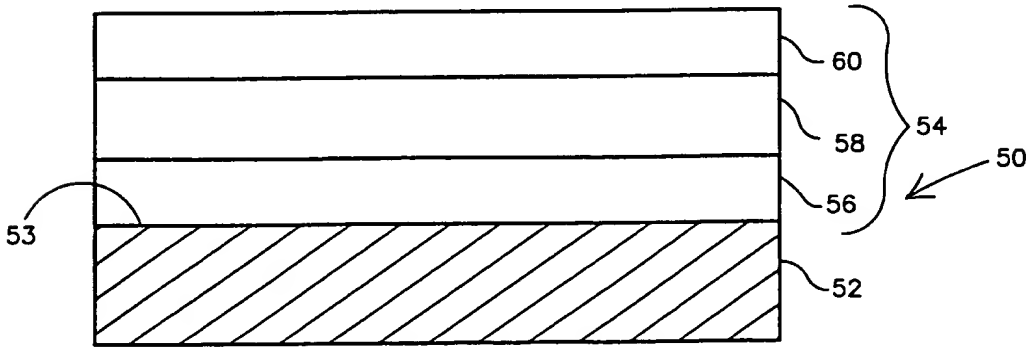


FIGURE 4

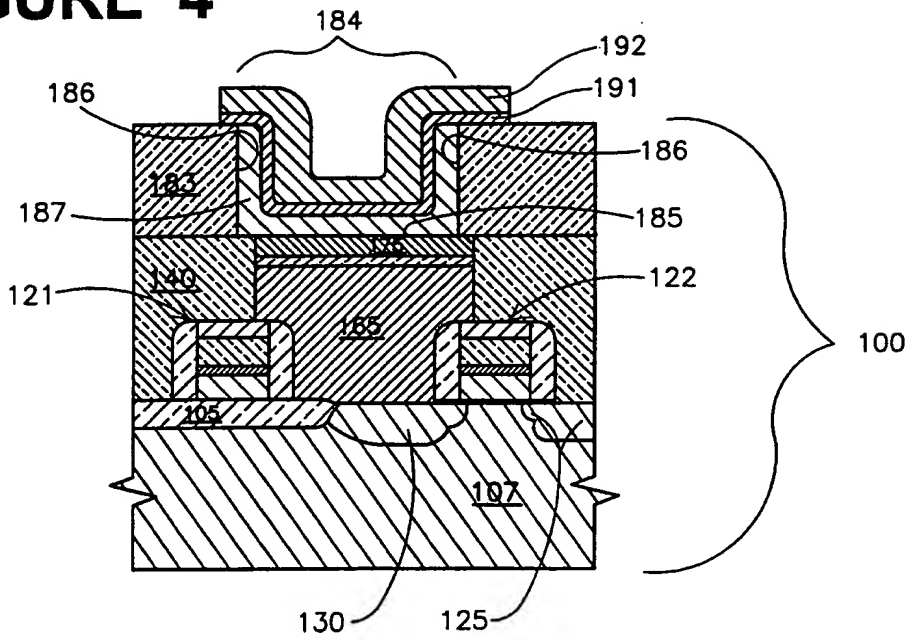


FIGURE 5

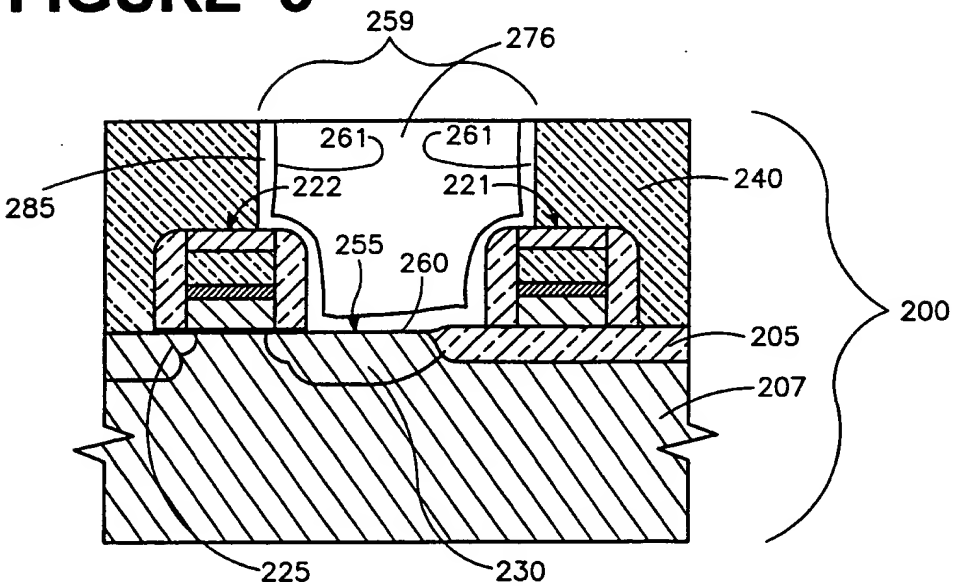


FIGURE 6A

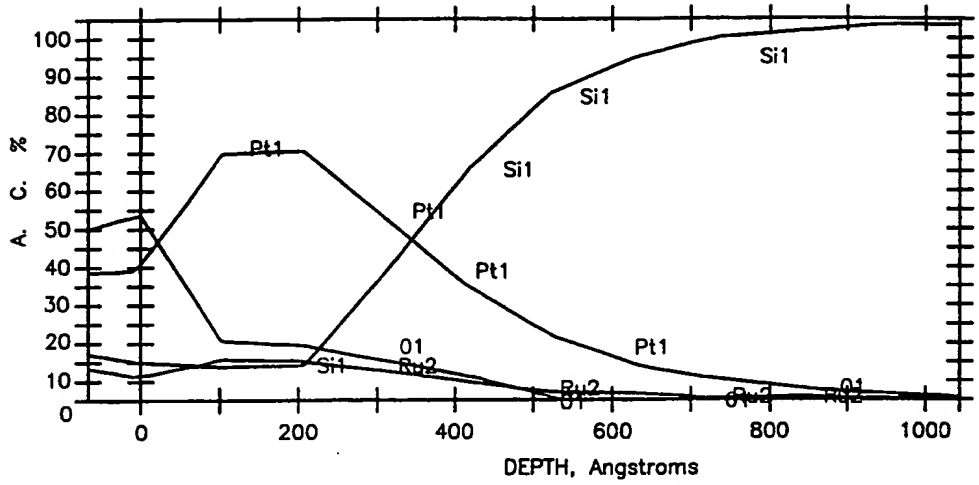


FIGURE 6B

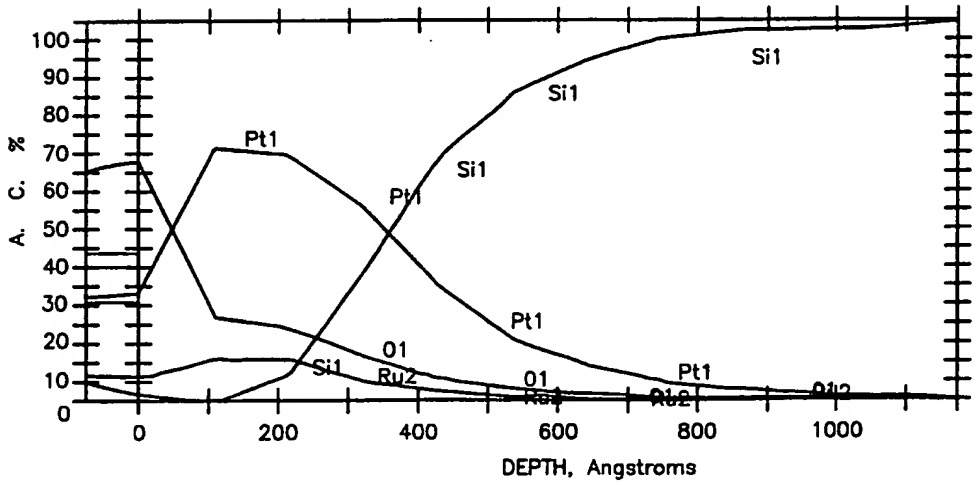
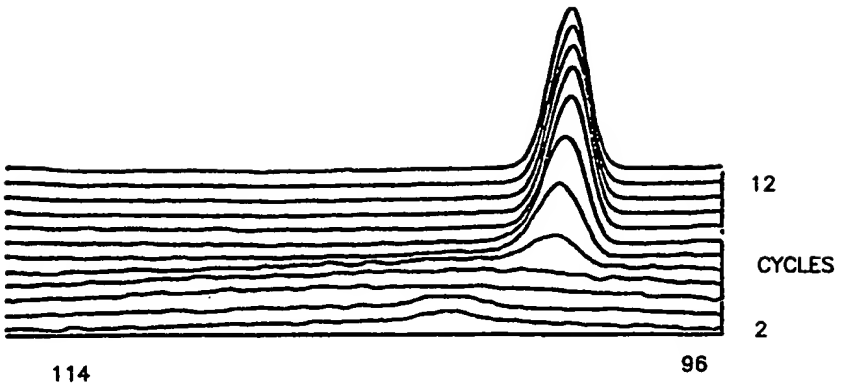


FIGURE 6C



INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/20053

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/02 H01L21/768 H01L21/285 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 714 402 A (CHOI KYEONG KEUN) 3 February 1998 (1998-02-03)	6,11, 17-19, 27,30-34
Y		10,14,20
A	column 2, line 19 -column 4, line 5; claim 1; figure 7	37
Y	US 5 696 384 A (OGI KATSUMI ET AL) 9 December 1997 (1997-12-09)	10,14,20
A	column 2, line 19 - line 28	4
Y	US 5 372 849 A (MCCORMICK FRED B ET AL) 13 December 1994 (1994-12-13) cited in the application	10,14,20
A	the whole document	4

-/—

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 December 1999	11/01/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Micke, K

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/20053

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	AL-SHAREEF H N ET AL: "Analysis of the oxidation kinetics and barrier layer properties of ZrN and Pt/Ru thin films for DRAM applications" THIN SOLID FILMS,CH,ELSEVIER-SEQUOIA S.A. LAUSANNE, vol. 280, no. 1, page 265-270 XP004008444 ISSN: 0040-6090 page 265, right-hand column, paragraph 2 -page 266, right-hand column, paragraph 1 page 268, right-hand column, paragraph 2 -page 269, left-hand column, paragraph 4 page 270, left-hand column, paragraph 2 -right-hand column, paragraph 1; figures 1,8	1-39
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P,A	column 1, line 37 -column 3, line 10 column 4, line 28 - line 33 column 5, line 3 - line 5	38,39

1

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